

FIG. 1

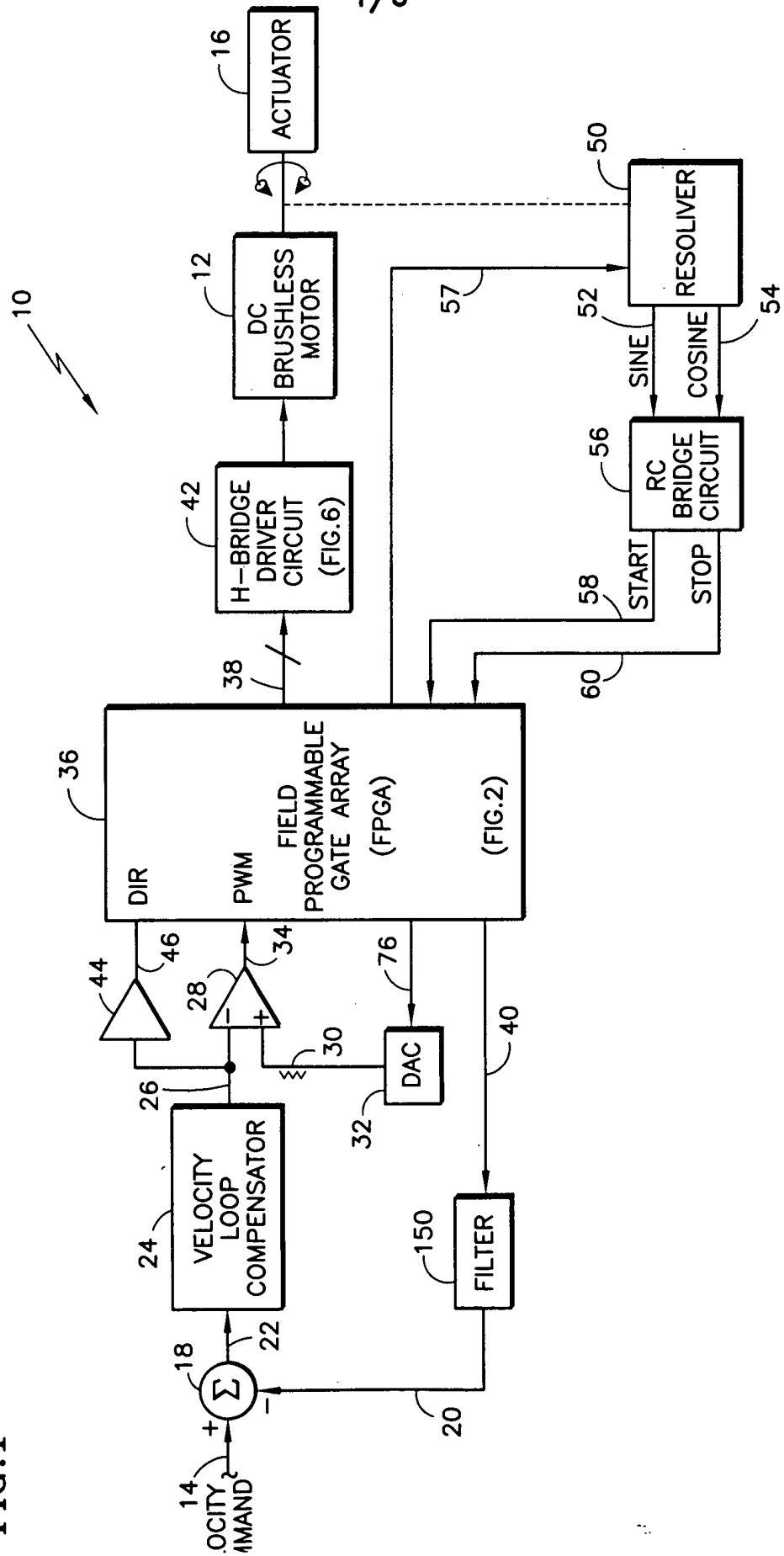
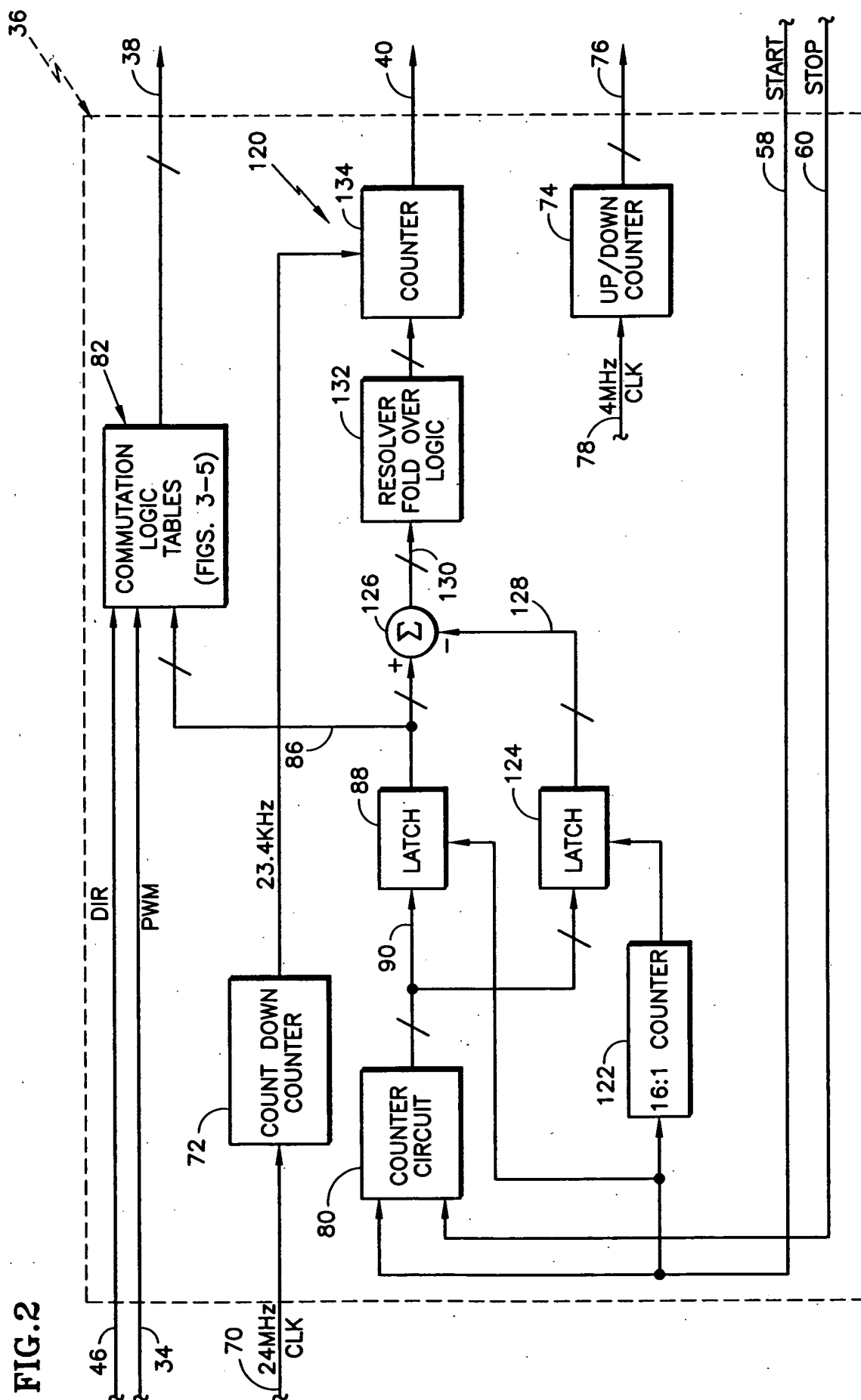
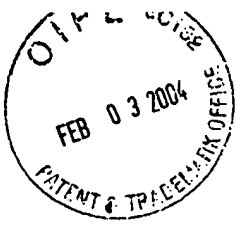


FIG. 2

The diagram illustrates a digital signal processing system. It begins with two input signals, 46 and 34, which are fed into a block labeled 82, "COMMUTATION LOGIC TABLES (FIGS. 3-5)". This block also receives a "DIR" signal. The output of block 82 is a "PWM" signal, which is fed into a "COUNT DOWN COUNTER" (72). The counter 72 is clocked by a "24MHz CLK" signal (70) and produces a "23.4KHz" output (86). This 23.4KHz signal is fed into a "COUNTER CIRCUIT" (80). The output of the counter circuit (80) is fed into a "LATCH" (88). The output of latch 88 is fed into a "SUM" block (126), which also receives a "+" input from the 23.4KHz signal (86) and a "-" input from a "16:1 COUNTER" (122). The output of the sum block (126) is fed into a "RESOLVER FOLD OVER LOGIC" block (132). The output of block 132 is fed into a "COUNTER" (134). The output of counter 134 is fed into an "UP/DOWN COUNTER" (74). The output of the up/down counter (74) is fed into a "START" signal (58) and a "STOP" signal (60). The output of the 16:1 counter (122) is fed into a "LATCH" (124). The output of latch 124 is fed into the "SUM" block (126). The output of the sum block (126) is also fed into the "RESOLVER FOLD OVER LOGIC" block (132). The output of the resolver fold over logic block (132) is fed into the "COUNTER" (134). The output of the counter (134) is fed into the "UP/DOWN COUNTER" (74). The output of the up/down counter (74) is fed into the "START" signal (58) and the "STOP" signal (60).



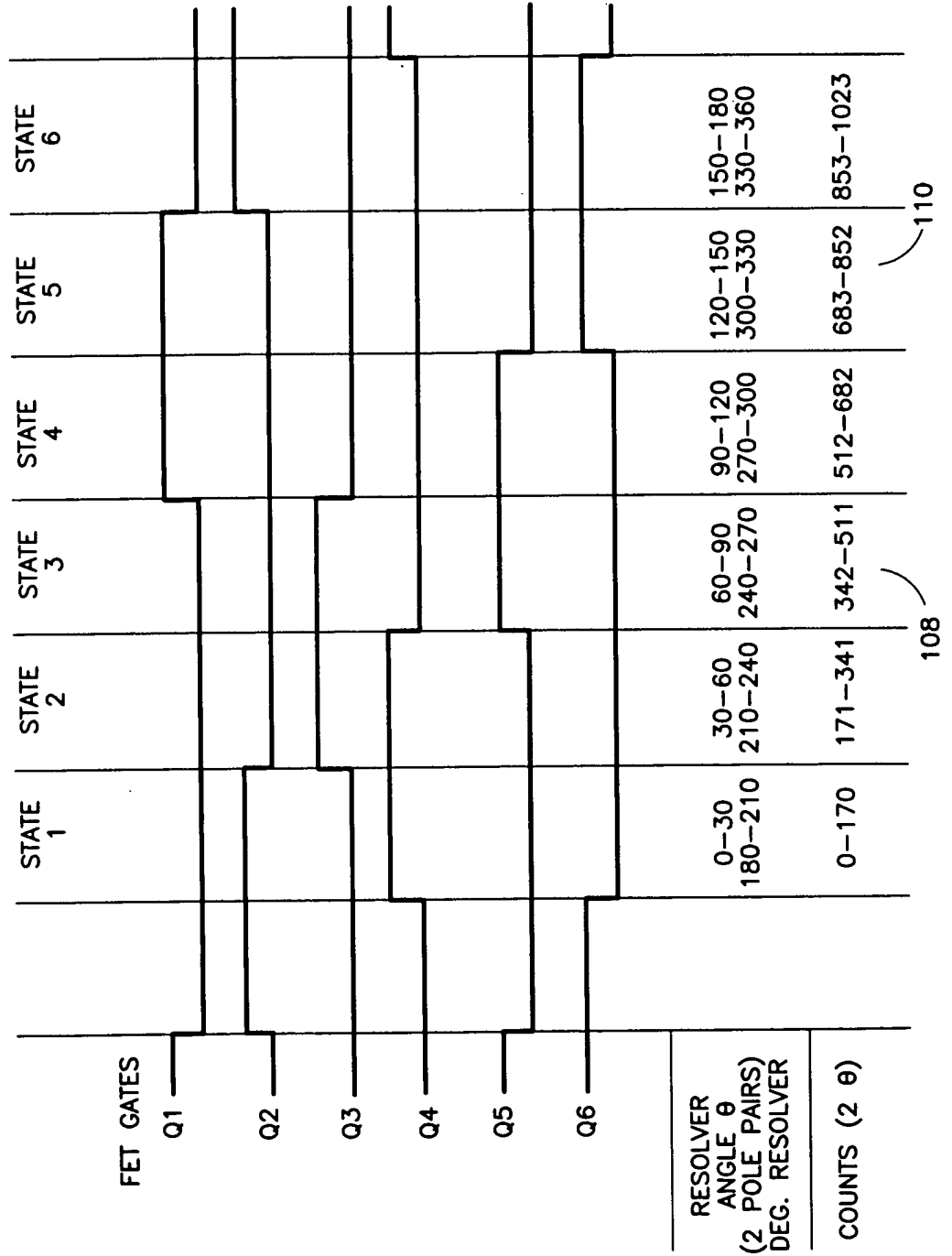


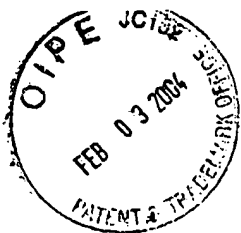
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CASE: PWM=1
DIR=1

82

FIG.3





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CASE: PWM=1
DIR=0

82

IG.4

	STATE 1	STATE 2	STATE 3	STATE 4	STATE 5	STATE 6	
FET GATES							
Q1							
Q2							
Q3							
Q4							
Q5							
Q6							
RESOLVER ANGLE θ (2 POLE PAIRS) DEG. RESOLVER	0-30 180-210	30-60 210-240	60-90 240-270	90-120 270-300	120-150 300-330	150-180 330-360	
COUNTS (2 θ)	0-170	171-341	342-511	512-682	683-852	853-1023	

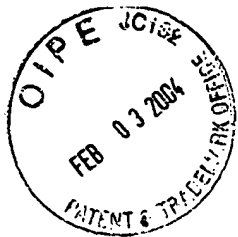


FIG. 5

CASE: PWM=0
DIR=0 OR 1

DIR = 1 PWM = 0
DIR = 0 PWM = 0

FET GATES	STATE 1	STATE 2	STATE 3	STATE 4	STATE 5	STATE 6	
Q1 0							
Q2 0							
Q3 0							
Q4 1							
Q5 1							
Q6 0							
RESOLVER ANGLE θ (2 POLE PAIRS) DEG. RESOLVER	0-30 180-210	30-60 210-240	60-90 240-270	90-120 270-300	120-150 300-330	150-180 330-360	
COUNTS (2 θ)	0-170	171-341	342-511	512-682	683-852	853-1023	

FIG.6

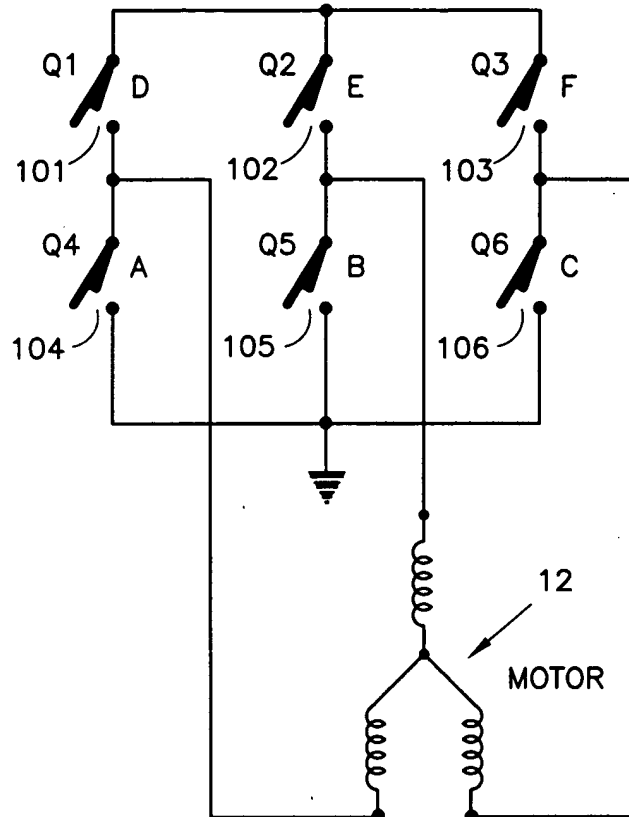


FIG.7

132

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IF MAGNITUDE > 180 DEG. ELEC.
  IF SIGN IS NEG, ADD 360 DEG. ELEC.
ELSE
  IF SIGN IS POS, SUBTRACT 360 DEG. ELEC.
ELSE
  OUTPUT = INPUT
  
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